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10/063,793	05/14/2002	Kuo-Tso Chen	8192-US-PA	1583

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,793	CHEN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,8,10-12,15,18-20,23-25,28* is/are rejected.

7)☒ Claim(s) *2,6,7,9,13,14,16,17,21,22,26,27,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: two sheets from Internet site xreferplus.com containing definitions of "circuit.".

DETAILED ACTION

1. The present Office Action is responsive to Applicant's remarks in the Response filed May 25, 2005. Claims 1-30 remain pending in the instant Application.

Claim Objections

2. Claims 1 and 15 are objected to because of the following informalities:

In Claim 1, line 10: "corresponded" should be changed to --corresponding--.

In Claim 15, line 12: "is deposited by" should be changed to --are deposited with a--.

Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

(i) Mowatt et al. (US 6,400,573 A1)

(ii) Fillion et al. (US 5,315,486)

(iii) Two sheets, each having a definition of a "circuit;" one from the *Newnes Dictionary of Electronics* (Newnes 1999) and the other from *Hargrave's Communications Dictionary* (Wiley 2001), as found on the Internet at xreferplus.com.

(iv) Wachtler et al. (US 6,274,391 B1)†

†Previously made of record in the instant Application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 5, 8, 12, 15, 20, 23 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Mowatt et al.

As to Claims 1 and 8, Mowatt et al. discloses, in Figs. 4 and 6: a substrate (Fig. 4) having a first (upper) surface, wherein the substrate comprises an internal circuit 18 (col.5: 3-4 and 6-8); a chip 56 having an active surface with a plurality of bonding pads 62, 64 thereon (Figs. 4 and 6; note that in Fig. 6, the bonding pad referenced as "60" should have been numbered 64) and a backside surface attached to the first (upper) surface of the substrate (col.6: 14-17; Fig. 4 shows that the first surface includes a cavity 14 into which chip 56 is mounted, the exposed floor of the cavity 14 being a part of the upper--i.e., first--surface of the substrate and having the chip 56 attached thereto using adhesive 58); and a build-up circuit structure on the substrate (Fig. 6), the build-up circuit structure having at least one insulation layer 126, at least one patterned circuit layer (col.8: 28-33) and a plurality of via openings (col.8: 15-16), wherein the insulation layer 126 is located between the active surface of chip 56 and the patterned circuit layer

(Fig. 6 and col.8: 28-33), the via openings corresponding to the bonding pads 62 and 64 (bonding pad 64 mislabeled as "60" in Fig. 6) pass through insulation layer 126 (Fig. 6; col.8: 15-16), wherein the via openings are deposited with a conductive material 130, 132 (Fig. 6; col.8: 15-17 and 22-23), the patterned circuit layer electrically connects with the bonding pads 62, 64 through the conductive material 130, 132 (col.8: 28-33) and a portion of the patterned circuit layer expands into a region outside the active surface of the chip 56 (in order to, for example, connect to another chip or another circuit point on the surface of insulation layer 126 that carries the patterned circuit layer, as taught in col.8: 28-33).

As to Claims 5 and 12, Mowatt et al. further discloses the substrate is formed of polymer material (col.3: 11-21 and col.4: 26-32).

As to Claims 15 and 23, Mowatt et al. discloses, in Figs. 4 and 6: a substrate (Fig. 4) having a first surface and at least one cavity 14 located on the first surface of the substrate (Fig. 4), wherein the substrate comprises an internal circuit 18 (col.5: 3-4 and 6-8); at least one chip 56 having an active surface with a plurality of bonding pads 62, 64 thereon (Figs. 4 and 6; note that in Fig. 6, the bonding pad referenced as "60" should have been numbered 64) and a backside surface attached to the bottom of the cavity 14 (Fig. 4; col.6: 14-17); and a build-up circuit structure on the substrate (Fig. 6), the build-up circuit structure having at least one insulation layer 126, at least one patterned circuit layer (col.8: 28-33) and a plurality of via openings (col.8: 15-16), wherein the insulation layer 126 is located between the active surface of chip 56 and the patterned circuit layer (Fig. 6 and col.8: 28-33), the via openings corresponding to the

bonding pads 62 and 64 (bonding pad 64 mislabeled as "60" in Fig. 6) pass through insulation layer 126 (Fig. 6; col.8: 15-16), wherein the via openings are deposited with a conductive material 130, 132 (Fig. 6; col.8: 15-17 and 22-23), the patterned circuit layer electrically connects with the bonding pads 62, 64 through the conductive material 130, 132 (col.8: 28-33) and a portion of the patterned circuit layer expands into a region outside the active surface of the chip 56 (in order to, for example, connect to another chip or another circuit point on the surface of insulation layer 126 that carries the patterned circuit layer, as taught in col.8: 28-33).

As to Claims 20 and 28, Mowatt et al. further discloses the substrate is formed of polymer material (col.3: 11-21 and col.4: 26-32).

6. Claims 1, 5, 8, 12, 15, 20, 23 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Fillion et al.

As to Claims 1 and 8, Fillion et al. discloses, in Fig.2: a substrate 16 (Fig. 4) having a first surface 18, wherein the substrate comprises an internal circuit 42 (col.5: 66-col.6: 3); a chip 22 having an active surface with a plurality of bonding pads 24 thereon (col.4: 36-40) and a backside surface attached to the first surface of the substrate (col.4: 51-61); and a build-up circuit structure 26 on substrate 16 (col.4: 62-68), the build-up circuit structure having at least one insulation layer 28 (col.4: 68-col.5: 9), at least one patterned circuit layer 32 (col.5: 24-38) and a plurality of via openings 30 (col.5: 12-15), wherein the insulation layer 28 is located between the active surface of chip 22 and the patterned circuit layer 32 (Fig. 2; col.8: 1-2, 5-9 and 20-28), the via openings 30 corresponding to the bonding pads 24 pass through insulation layer 28

(Fig. 2; col.5: 12-15), wherein the via openings are deposited with a conductive material (part of the patterned metallization layer 32; col.5: 20-23), the patterned circuit layer 32 electrically connects with the bonding pads 24 through the conductive material (col.5: 20-23) and a portion of the patterned circuit layer 32 expands into a region outside the active surface of the chip 22 (Fig. 2; col.5: 20-28).

As to Claims 5 and 12, Fillion et al. further discloses the substrate 16 is formed of metal (oxidized, or, a nitride compound; col.4: 29-30).

As to Claims 15 and 23, Fillion et al. discloses, in Fig.2: a substrate 16 (Fig. 4) having a first surface 18 and at least one cavity 20 located on the first surface 18 of the substrate (col.4: 36-42), wherein the substrate comprises an internal circuit 42 (col.5: 66-col.6: 3); at least one chip 22 having an active surface with a plurality of bonding pads 24 thereon (col.4: 36-40) and a backside surface attached to the bottom of cavity 20 (col.4: 51-61); and a build-up circuit structure 26 on substrate 16 (col.4: 62-68), the build-up circuit structure having at least one insulation layer 28 (col.4: 68-col.5: 9), at least one patterned circuit layer 32 (col.5: 24-38) and a plurality of via openings 30 (col.5: 12-15), wherein the insulation layer 28 is located between the active surface of chip 22 and the patterned circuit layer 32 (Fig. 2; col.8: 1-2, 5-9 and 20-28), the via openings 30 corresponding to the bonding pads 24 pass through insulation layer 28 (Fig. 2; col.5: 12-15), wherein the via openings are deposited with a conductive material (part of the patterned metallization layer 32; col.5: 20-23), the patterned circuit layer 32 electrically connects with the bonding pads 24 through the conductive material (col.5:

20-23) and a portion of the patterned circuit layer 32 expands into a region outside the active surface of the chip 22 (Fig. 2; col.5: 20-28).

As to Claims 20 and 28, Fillion et al. further discloses the substrate 16 is formed of metal (oxidized, or, a nitride compound thereof; col.4: 29-30).

7. Claims 1, 3-5, 8, 10-12, 15, 18-20, 23-25 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Wachtler et al. *Examiner's Note*: the dictionary definitions provided hereinbelow for the word "circuit" are included as part of the rejection of Claims 1, 8, 15 and 23 in accordance with multiple reference 35 USC § 102 rejections provided for in MPEP § 2131.01, part II.

A) As to Claims 1 and 8:

I. Wachtler et al. discloses: a substrate 12 having a first surface (Fig. 8; bottom surface of cavity 14); a chip 16 having an active surface with a plurality of bonding pads thereon (col.8: 63-67) and a backside surface attached to the first surface of substrate 12 (Fig. 9); and a build-up circuit structure 18 on substrate 12 (Fig. 22), the build-up structure having at least one insulation layer 24 and 26 (Figs. 10-12; col.9: 1-18), at least one patterned circuit layer 34 and a plurality of via openings 28 and 40 (col.9: 19-40; Figs. 14-22), wherein the at least one insulation layer 24 and 26 is located between the active surface and the patterned circuit layer 34 (Fig. 14), the via openings 28 corresponding to the bonding pads pass through the at least one insulation layer 24 and 26 (Fig. 12; col.9: 19-23), wherein the via openings 28 are deposited with a conductive material 30, the at least one patterned circuit layer 34 electrically connects with the bonding pads through the conductive material 30 (which, after patterning, form the via

filling material 32 as well as the circuit layer 34) [col.9: 19-40] and a portion of the at least one patterned circuit layer 34 expands into a region outside the active surface of the chip (Figs. 14 and 22 show only one portion of the patterned circuit layer 34 expanded to a region outside the active surface of the chip, Figs. 7 and 26 show the inherent expansion of the *entirety* of the at least one patterned circuit layer 34 throughout the high density interconnect overlay 18, including a region outside the active surface of the chip, and col.9: 32-40); Wachtler et al. further discloses, in the embodiment of Fig. 31, that substrate 12 comprises a conductive path 58 (i.e., a conductive through-hole) built through--hence, internal to--the substrate to allow an alternative electrical path off the back side of the substrate in order to establish connections to other electronic devices, such as a printed wiring board (col.12: 24-38). In the electronics art, there exist various definitions of a "circuit" that admit the broad interpretation of a circuit as being simply a conductive path. Some of these exemplary definitions of a "circuit" obtained from sources on the Internet are: 1) "A path consisting of a conductor or a system of conductors through which an electric current can flow" (*Newnes Dictionary of Electronics*, Newnes 1999); 2) "Any path that can carry an electric current" (*Hargrave's Communications Dictionary*, Wiley 2001) [See attached sheets which includes these definitions of a "circuit," as found on the Internet at xreferplus.com]. Accordingly, the conductive path 58 built through--hence, internal to--the substrate 12 meets the Applicant's broad limitation of "the substrate comprises an internal circuit."

As to Claims 3, 10 and 11, Wachtler et al. further discloses: a plurality of solder ball pads 44 on the at least one patterned circuit layer 34 (Figs. 19 and 20); and a plurality of solder balls 22 attached to the solder ball pads, respectively (Fig. 21) [col.10: 26-27].

As to Claim 4, Wachtler et al. further discloses a passivation layer 46 disposed on the at least one patterned circuit layer 34, wherein the passivation layer 46 has a plurality of openings corresponding to solder ball pads 44 (Fig. 21; col.10: 23-26).

As to Claims 5 and 12 Wachtler et al. further discloses that substrate 12 is a plastic (i.e., polymer) material (col.8: 37-43).

F) As to Claims 15 and 23:

I. Wachtler et al. discloses: a substrate 12 having a first surface and at least one cavity 14 located on the first surface of the substrate (Fig. 8); a chip 16 having an active surface with a plurality of bonding pads thereon (col.8: 63-67) and a backside surface attached to the bottom of cavity 14 (Fig. 9); and a build-up circuit structure on substrate 12 (Fig. 22), the build-up structure having at least one insulation layer 24 and 26 (Figs. 10-12; col.9: 1-18), at least one patterned circuit layer 34 and a plurality of via openings 28 and 40 (col.9: 19-40; Figs. 14-22), wherein the at least one insulation layer 24 and 26 is located between the active surface and the patterned circuit layer 34 (Fig. 14), the via openings 28 corresponding to the bonding pads pass through the at least one insulation layer 24 and 26 (Fig. 12; col.9: 19-23), wherein the via openings 28 are deposited with a conductive material 30, the at least one patterned circuit layer 34 electrically connects with the bonding pads through the conductive material 30 (which,

after patterning, form the via filling material 32 as well as the circuit layer 34) [col.9: 19-40] and a portion of the at least one patterned circuit layer 34 expands into a region outside the active surface of the chip (Figs. 14 and 22 show only one portion of the patterned circuit layer 34 expanded to a region outside the active surface of the chip, Figs. 7 and 26 show the inherent expansion of the *entirety* of the at least one patterned circuit layer 34 throughout the high density interconnect overlay 18, including a region outside the active surface of the chip, and col.9: 32-40). Wachtler et al. further discloses, in the embodiment of Fig. 31, that substrate 12 comprises a conductive path 58 (i.e., a conductive through-hole) built through--hence, internal to--the substrate to allow an alternative electrical path off the back side of the substrate in order to establish connections to other electronic devices, such as a printed wiring board (col.12: 24-38). In the electronics art, there exist various definitions of a "circuit" that admit the broad interpretation of a circuit as being simply a conductive path. 1) "A path consisting of a conductor or a system of conductors through which an electric current can flow" (*Newnes Dictionary of Electronics*, Newnes 1999); 2) "Any path that can carry an electric current" (*Hargrave's Communications Dictionary*, Wiley 2001) [See attached sheets which includes these definitions of a "circuit," as found on the Internet at xreferplus.com]. According to these broad definitions of a "circuit," the conductive path 58 built through--hence, internal to--the substrate 12 meets the Applicant's broad limitation of "the substrate comprises an internal circuit."

As to Claims 18, 24 and 25, Wachtler et al. further discloses: a plurality of solder ball pads 44 on the at least one patterned circuit layer 34 (Figs. 19 and 20); and a

plurality of solder balls 22 attached to the solder ball pads, respectively (Fig. 21) [col.10: 26-27].

As to Claim 19, Wachtler et al. further discloses a passivation layer 46 disposed on the at least one patterned circuit layer 34, wherein the passivation layer 46 has a plurality of openings corresponding to solder ball pads 44 (Fig. 21; col.10: 23-26).

As to Claims 20 and 28, modified Wachtler et al. further discloses that substrate 12 is a plastic (i.e., polymer) material (col.8: 37-43).

Allowable Subject Matter

8. Claims 2, 6-7, 9, 13-14, 16, 17, 21-22, 26, 27 and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

10. Applicant's arguments on pp.2-3 of the Response filed May 25, 2005, with respect to the rejection(s)of claim(s) 1, 3-8, 10-15, 18-25 and 28-30 under 35 USC § 103(a) over Wachtler et al. in view of Viswanathan et al., have been fully considered and are, to a limited extent, persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of a new interpretation of the previously applied Wachtler et al. (US 6,274,391 B1), as well as newly found prior art. Also, Applicant's arguments on p.4 of the Response filed May 25, 2005, with respect to the rejections of Claims 1-30 under 35 USC § 103(a) over Cheng et al. in view of Wachtler et al. and Viswanathan et al. (in conjunction with the *Accuratus* data sheets on alumina and aluminum nitride), have been fully considered and are, to a limited extent, persuasive:

A) Further to the Applicant's arguments on pp.2-3, the Examiner now sees that the substrate/cover of Viswanathan et al. (US 6,724,079 B2) is not comparable to the substrate of Wachtler et al. The substrate/cover 140 of Viswanathan et al. does not have a built-up circuit structure (only the chip 130 has the built-up multilayer circuit structure 124; col.3: 39-43) while the substrate 12 of Wachtler et al. has a built-up multilayer circuit structure 18 that provides all or most of the interconnection circuitry for the package assembly. That is the main difference between the package assemblies of Viswanathan et al. and Wachtler et al. The extensive internal circuitry of the Viswanathan et al. substrate/cover 140 is necessary to the package assembly since the support substrate 110 only functions as a mechanical support and heat sink for the chip and substrate/cover; substrate 110 is not contemplated as an electrical interconnect. Therefore, substrate/cover 140 is left to provide the extensive circuitry necessary for the package assembly. Since the substrate 12 of Wachtler et al. already has the required interconnection circuitry for the package assembly provided by the built-up circuit structure 18, then it would not be obvious to yet further modify the substrate 12

Wachtler et al. with the extensive interconnection circuitry of Viswanathan et al. since the built-up circuit structure 18 of Wachtler et al. already provides the contemplated interconnection circuitry for the package assembly. There is no teaching or suggestion in Wachtler et al. that any extensive circuitry additional to the built-up interconnections circuit structure 18 is required or for the electronic functions and applications contemplated for the package assembly disclosed. Accordingly, the Examiner concedes that further modifying the substrate 12 of Wachtler et al. with additional extensive internal substrate circuitry, as taught in the structurally different Viswanathan et al. would not be obvious in view of the extensive built-up interconnection circuitry already-existing on the substrate 12 of Wachtler et al. for providing the necessary electrical interconnections. Accordingly, the Examiner has withdrawn the rejection of Claims 1, 3-8, 10-15, 18-25 and 28-30 under 35 USC § 103 based on Wachtler et al. in view of Viswanathan et al. for the reasons given above.

B) Similarly, and further to the Applicant's arguments on p.4, in Cheng et al. (US 2003/0134455 A1) wherein the disclosed support substrate 300 already has the built-up interconnect structure thereon (Figs. 14-24), it is neither taught nor suggested that any further circuit modification be made to substrate 300 (disclosed as a metal plate) for enhancing the circuit function of the package, and the Examiner accordingly concedes that it would not be obvious to further modify the substrate of Cheng et al. with the extensive internal substrate interconnection circuitry of the (alumina or aluminum nitride) substrate/cover in Viswanathan et al., the Viswanathan et al. substrate/cover having no built-up circuitry on a surface thereof and the extensive internal circuit providing the only

interconnect circuitry in its package assembly, quite distinct from the operational structure disclosed in Cheng et al. Accordingly, the Examiner has withdrawn the rejection of Claims 1-30 under 35 USC § 103 based on Cheng et al. in view of Wachtler et al. and Viswanathan et al. because the Examiner now takes the position that it would not be obvious to further modify the substrate in Cheng et al. with the extensive internal substrate circuit of Viswanathan et al. for the reasons given above.

C) However, the Examiner has taken a second look at the embodiment of Figs. 30 and 31 in Wachtler et al. and has now determined that the conductive path 58 (Fig. 31), which is a through-hole in substrate 12, in fact constitutes a "circuit" in the broadest sense of the word, as used in the electronics art, and since the conductive path 58 is a through-hole--i.e., a conductive path within the substrate--it constitutes an "internal circuit" as broadly claimed in Applicant's Claims 1, 8, 15 and 23. The Examiner has provided two examples of broad definitions of "circuit" found in two electronics dictionaries to support his interpretation of "circuit." Accordingly, Claims 1, 3-5, 8, 10-12, 15, 18-20, 23-25 and 28 now stand as rejected over Wachtler et al., in conjunction with the dictionary definitions of "circuit," under 35 USC § 102(e).

D) Due to the new ground(s) of rejection made in view of a new interpretation of the previously applied Wachtler et al. (US 6,274,391 B1), as well as newly found prior art, the present Office Action is made NON-FINAL.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Eichelberger (US 5,111,278) discloses a base substrate 30 having internal conductive paths 32 (i.e., internal circuit) and a built-up multilayer circuit thereon (Fig. 2; col.8: 43-68).

b) Ogawa et al. (JP2000-260902 A) discloses a substrate base substrate 2 having internal conductive paths 8 (i.e., internal circuit) and a built-up multllayer circuit thereon (Fig. 1).

c) Yamagishi (JP10-284632 A) discloses a base substrate 114 having internal circuitry and a substrate 41 comprising a built-up multilayer circuit 111 (Fig. 5c) thereon and internal conductive paths 44a,b (i.e., internal circuit), the substrate 41 mounted in a cavity in base substrate 112 (Fig. 5a).

d) Cole, Jr. et al. (US 5,157,589) discloses a base substrate 12 having a built-up multilayer circuit structure thereon comprising layers 20, 30 and 40 (Fig. 3), the built-up circuit structure providing the electrical interconnections in the package assembly (col.9: 67-col.11: 2).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
August 16, 2005